REMARKS/ARGUMENTS

These remarks are made in response to the Advisory Action of February, 18, 2005 sent in response to the reply to the Final Office Action of September 20, 2004. This response is timely filed with a one-month request for a retroactive extension of time and the appropriate fees.

In the Advisory Action, the Examiner indicated that the Application was not in a condition for allowance as then claimed. The Examiner further indicated that certain features not claimed for which arguments were presented did distinguish the application from cited art, and amendments including such arguments if supported by the specification may be sufficient to overcome the prior art of record.

During a telephone interview with the Examiner on February 22, 2005, the Examiner clarified for the Applicants that the mentioned distinction centered on strengthening the linkages between the local memories of the various processors modules and the language model cache memory. Applicants have attempted to amend the claims, in a manner supported by the specification that clarifies this linkage in the claims.

That is, Applicants have amended independent claims 1, 17, 18, 20, and to clarify that a portion of local memory for each of the multiple processor modules is allocated as a local language module cache for locally storing data extracted from the language model cache. Each of the multiple processor modules can selectively utilize the local language module cache to minimize traffic between the multiple processor modules and the language model cache when executing loaded speech allocation tasks.

The amendment is supported by claims 18 and 19 (as originally written), page 18, lines 1-4, lines 6-9, page 17, lines 6-10, page 22, lines 19-21, page 19, lines 1-2, page 16, lines 2-4, page 13, lines 13-20, page 12, lines 18-20, page 9, lines 6-8, by FIG. 1 and 2, and throughout the specification.

More specifically, page 17, lines 6-10 states that each processor module 102 can have local memory available for use by loaded speech application tasks and that each

processor module 102 can access remote language model caches. Page 18, lines 7-9 states that a substantial portion of local memory 204 of each processor module 102 can be allocated as a language model cache, in order to further reduce traffic in the local communications bus 104. As state on page 19, lines 12-14, the language model cache 106B can be mapped to a common address space where the language model cache 106 can be uniformly accessed by all processor modules 102 in the speech processing board 100. Further, page 19, lines 17-19 states that each language model can be stored contiguously in memory. During the boot strap load process performed by each processor module 102, a uniform starting address can be provided to the processor module.

Since the amendment is properly supported by the specification, no new matter results from these claim amendments.

Applicants believe the amendments to the independent claims distinguish the Application from cited art, thereby placing the application in full condition for allowance, which action is respectfully requested. Applicants request that the Examiner call the undersigned if clarification is needed on any matter within this Amendment, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

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